REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 1-9, 13-16, 20-23 and 25-27 are present in this application, claim 24 being canceled by way of the present amendment. Claims 3-9 are withdrawn. Amended claims 1, 15 and 27 are supported by Fig. 1. No new matter is believed to be added.

Claims 1 and 24 were objected to in paragraphs 4 and 5 of the Office Action. Claim 1 is amended as requested, and claim 24 is canceled.

Claims 1 and 22-24 are rejected under 35 U.S.C. § 102(e) over Anderson. Under 35 U.S.C. § 103(a), claims 2, 13-16, 20, 21, 25 and 27 are rejected over Anderson in view of U.S. 6,400,471 (Kuo et al.), and claim 26 is rejected over Anderson and Kuo et al. in view of U.S. 6,002,446 (Eglit).

Each of the image processing apparatuses of claims 1, 15 and 27 includes an image processing part and a compression unit. The apparatus of claims 1 and 27 also includes a buffer memory and the apparatus of claim 15 includes two buffer memories. The buffer memories store image data. The claims are clarified as to the connections of the buffer memory (or memories). The buffer memory (or memories) is (are) not connected to the bus, the input of said buffer memory is connected only to said image processing unit to receive only said image data from said image processing unit, and the output of said buffer memory is connected only to said compression unit to output said image data only to said compression unit. The separate connections provide for reduced transfers between the storage unit and the image processing part.

Turning to the prior art rejections, Anderson discloses an image processing system having an image processing data path 202 to convert raw image data into real image data capable of being displayed. Path 202 is connected to MCU buffer 204, buffer 204 being used to coordinate the transfer of displayable image data to the JPEG block 205. Data can also be

sent from buffer 204 to resize block 206, YCC shuffle 208 or draw buffer 214, as described in columns 4 and 5 and shown in Figures 2A, 2B, 3A, and 3B. Also, data may be input to buffer 204 from draw buffer 214, as illustrated in Figure 2B. The system of Anderson also includes a bus 113 to which various components are connected.

In the image processing apparatus of claim 1, the buffer memory is not connected to the bus, the input of the buffer memory is connected only to the image processing unit to receive only the image data from the image processing unit, and the output of the buffer memory is connected only to the compression unit to output the image data only to the compression unit. In contrast, as illustrated in Figures 2A and 2B of Anderson, buffer 204 receives data from path 202, shuffle 208, or from path 202 and buffer 214. Also, buffer 204 outputs data to JPEG 205 and resize block 206 (Figure 2A) or to resize block 206 and draw buffer 214 (Figure 2B). The buffer 214, asserted to correspond to the buffer memory, is clearly not connected such that the input only receives data from an image processing unit and the output is only connected to a compression unit to output image data only to the compression unit. The buffer 204 of Anderson receives data from multiple sources and outputs data to multiple sources. Anderson clearly does not disclose or suggest the image processing apparatus of claim 1.

The same is true for claim 15, where the inputs of the first and second buffer memories are connected only to the image processing unit to receive only the image data from the image processing unit, and the outputs of the first and second buffer memories are connected only to the compression unit to output the image data only to the compression unit. The buffer memories are not connected to the bus. Claim 15 is also not disclosed or suggested by Anderson.

Lastly, the buffer memory in claim 27 is not connected to the bus, the input of the buffer memory is connected only to the image processing unit to receive only image data

from the processing unit, and the output of the buffer memories connected only to the compression unit to output the image data only to the compression unit. Anderson does not disclose or suggest an image processing apparatus having such structure.

Kuo et al. is relied upon for teaching first and second buffer memories and the operation of the buffer memories. However, even if the system of Anderson can be modified to include two buffer memories that operate as described in Kuo et al., the combined system would still be connected as described above and, thus, would clearly not disclose or suggest the apparatuses as recited in claims 1, 15 or 27 for the respective reasons described above. Claims 1, 15 and 27 are patentable over a combination of Anderson and Kuo et al.

Eglit is cited for ping-pong buffers with a line width being greater than the line width of the memory. Even if such ping-pong buffers are included in the architectures of Kuo et al., the deficiencies noted above in Kuo et al. remain. The apparatuses of claims 1, 15 and 27 are neither taught nor suggested by a combination of Anderson, Kuo et al. and Eglit.

It is respectfully submitted the present application is in condition for allowance, and a favorable action to that effect is respectfully requested.

Respectfully submitted,

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